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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,357	06/23/2003	Robert Benware	02-6301 81563	8900

7590 09/23/2004

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EXAMINER	
RAYMOND, EDWARD	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,357	BENWARE, ROBERT	
	Examiner	Art Unit	
	Edward Raymond	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,9 and 11* is/are rejected.

7)☒ Claim(s) *2,4,6,8,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 3, 5, 7, 9, and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Verhelst et al. in view of Cole, Jr. et al. Verhelst et al. teach a method of screening defects comprising steps of (a) measuring a quiescent current at a first supply voltage for each of a plurality of devices (Claims 1 and 7: see col. 4, lines 30-38) and (b) measuring a quiescent current at a second supply voltage for each of the plurality of devices (Claims 1 and 7: see col. 4, lines 30-38).

Verhelst et al. teach a method wherein the first supply voltage is a nominal supply voltage of the plurality of devices (Claims 3 and 9: see col. 4, lines 55-64).

Verhelst et al. teach a method wherein the quiescent current is measured at the first supply voltage for multiple stop points in a test pattern (Claims 5 and 11: see col. 6, lines 1-13: The Examiner notes that the measurements at the multiple transistors is equivalent to multiple stop points in a test pattern).

Verhelst et al. does not teach (c) generating a plot of the quiescent current measured at the first supply voltage vs. the quiescent current measured at the second supply voltage for each of the plurality of devices; (d) determining a range of intrinsic variation of quiescent current in the plot; and (e) identifying any of the plurality of

devices corresponding to a measurement plotted outside the range of intrinsic variation as defective. Cole, Jr. et al. teach (c) generating a plot of the quiescent current measured at the first supply voltage vs. the quiescent current measured at the second supply voltage for each of the plurality of devices (Claims 1 and 7: see Figure 3 and also col. 8, lines 20-51: The Examiner notes that first supply voltage and second supply is plotted); (d) determining a range of intrinsic variation of quiescent current in the plot (Claims 1 and 7: see col. 10, lines 1-16); and (e) identifying any of the plurality of devices corresponding to a measurement plotted outside the range of intrinsic variation as defective (Claims 1 and 7: see col. 4, lines 47-63). It would have been obvious to the person having ordinary skill in the art at the time the invention was made to modify Verhelst et al. to use a plot to find the range of variation of quiescent current to identify defects, as taught by Cole, Jr. et al., because this would allow for adequately indicating whether a VLSI circuit under test is free from defects (see col. 1, lines 35-52).

Allowable Subject Matter

3. **Claims 2, 4, 6, 8, 10, and 12** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Raymond whose telephone number is 571-272-2221. The examiner can normally be reached on Monday through alternating Friday between 8:00 AM and 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-2221 for regular communications and 571-272-1562 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

September 17, 2004
Edward Raymond
Patent Examiner
Art Unit 2857

Edward Raymond
[redacted] Patent Examiner